Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. Claim 1 (currently amended) A semiconductor wafer comprising:

a substrate with a first region, a second region, and a third region horizontally defined on the surface thereof; and

a capacitor disposed on the substrate, the capacitor further comprising:

a first electrode disposed in the first region and the third region on the substrate;

a first isolation layer disposed on the first electrode, the first isolation layer covering a portion of the first electrode in the third region and the substrate in the second region, but not covering the first electrode in the first region; and

a second electrode disposed on the first isolation layer, the second electrode covering the first electrode in the third region and covering the substrate in the second region.

Claim 2 (previously presented) The semiconductor wafer of claim 1 wherein the capacitor further comprises a second isolation layer covering the capacitor and the substrate.

Claim 3 (original) The semiconductor wafer of claim 2 wherein the capacitor further comprises a first contact plug located in the second isolation layer and electrically connected to the first electrode.

Claim 4 (original) The semiconductor wafer of claim 3 wherein the first contact plug is located in the first region.

Claim 5 (original) The semiconductor wafer of claim 2 wherein the

capacitor further comprises a second contact plug located in the second isolation layer and electrically connected to the second electrode.

Claim 6 (original) The semiconductor wafer of claim 5 wherein the second contact plug is located in the second region or the third region.

Claim 7 (original) The semiconductor wafer of claim 1 wherein the semiconductor wafer further comprises a field oxide layer located beneath the first electrode.

Claim 8 (original) The semiconductor wafer of claim 1 wherein the first electrode comprises a polysilicon layer or a doped polysilicon layer.

Claim 9 (original) The semiconductor wafer of claim 1 wherein the second electrode comprises a polysilicon layer or a doped polysilicon layer.

Claim 10 (original) The semiconductor wafer of claim 1 wherein the first isolation layer comprises a silicon oxide layer or a silicon nitride layer.

Claim 11 (currently amended) A capacitor disposed on a substrate, the substrate having a first region, a second region, and a third region horizontally defined on the surface thereof, the capacitor comprising:

a first polysilicon layer disposed in the first region and the third region on the substrate;

a dielectric layer covering a portion of the first polysilicon layer in the third region and the substrate in the second region, but not covering the first polysilicon layer in the first region; and

a second polysilicon layer disposed on the dielectric layer, the second polysilicon layer covering the first polysilicon layer in

the third region and covering the substrate in the second region.

Claim 12 (original) The capacitor of claim 11 wherein the capacitor further comprises a first contact plug electrically connected to the first polysilicon layer.

Claim 13 (original) The capacitor of claim 12 wherein the first contact plug is located in the first region.

Claim 14 (original) The capacitor of claim 11 wherein the capacitor further comprises a second contact plug electrically connected to the second polysilicon layer.

Claim 15 (original) The capacitor of claim 14 wherein the second contact plug is located in the second region or the third region.

Claim 16 (original) The capacitor of claim 11 wherein the capacitor further comprises a field oxide layer located under the first polysilicon layer.